## ABSTRACT OF THE DISCLOSURE

The present invention provides an asynchronous FIFO apparatus and method for passing data between a first clock domain and a second clock domain of a data processing apparatus, the first clock domain being asynchronous with respect to the second clock domain. The asynchronous FIFO apparatus comprises a main FIFO memory operable to store the data to be passed between the first and second clock domains, the main FIFO memory being accessible from each clock domain under the control of an access pointer associated with that clock domain. For one or both of the clock domains, the amount of data accessible per clock cycle is variable. An auxiliary FIFO memory is also provided associated with each clock domain in which the amount of data accessible per clock cycle is variable, this auxiliary FIFO memory being operable to store the access pointer used to access the main FIFO memory from its associated clock domain, and the access pointer being stored at a location of the auxiliary FIFO memory specified by an auxiliary access pointer. Routing logic is then operable to pass the auxiliary access pointer to the other clock domain to enable that other clock domain to retrieve the access pointer stored in the auxiliary FIFO memory. This provides an efficient technique for enabling data to be passed between two asynchronous clock domains in situations where for at least one of the clock domains the amount of data accessible per clock cycle in the main FIFO memory is variable.